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T2R4_024_020

24-GHz Dual Transmitter / Quad Receiver MMIC

Preliminary Data Sheet

Status:	Date:	Author:	Filename:	
Final	2018-03-20	Silicon Radar GmbH	Datasheet_T2R4_024_020_V0.1	
Version:	Product number:	Package:	Marking:	Page:
0.1	T2R4_024_020	QFN32, 5 mm × 5 mm	T2R4 YYWW	1 of 21

Version Control

Version	Changed section	Description of change	Reason for change
0.1		Initial Release	

Table of Contents

1 Features

- Radar transceiver for 24-GHz ISM band
- Single supply voltage of 3.3 V
- Fully ESD protected device
- Low power consumption of 430 mW (4RX+1TX)
- Transmitters with power control in two steps
- Receivers with homodyne quadrature mixer
- Low-noise amplifiers (LNA) with gain control
- Integrated low phase noise push-push VCO
- Divider division ratio 1:8
- 2 single ended TX outputs
- 4 single ended RX inputs
- SPI interface
- QFN32 leadless plastic package $5 \times 5\ mm^2$
- Pb-free, RoHS compliant package

1.1 Overview

The IC is an integrated transceiver circuit for the 24-GHz ISM band in the frequency range 24.0 GHz – 24.25 GHz. It includes four receive and two transmit channels. Each of receive channels has a low-noise amplifier (LNA) with gain control, quadrature mixers, a poly-phase filter. Both transmit channels have a power amplifier with gain control. The circuit includes also a voltage controlled oscillator with two tuning inputs, a divide-by-8 circuit, and a SPI interface to control all sub-circuits. Each of the receivers can be powered down and the gain of the receiver can be digitally set to high gain mode or low gain mode. The output power of each transmitter can be digitally controlled and they can be powered down as well. The IC is fabricated in SiGe BiCMOS technology.

1.2 Applications

The TRX_024_007 can be used in in radar systems for the ISM band from 24.0 GHz to 24.25 GHz and for UWB applications between 23 GHz and 26 GHz. It can be used in radar systems with angular resolution.

2 Block Diagram

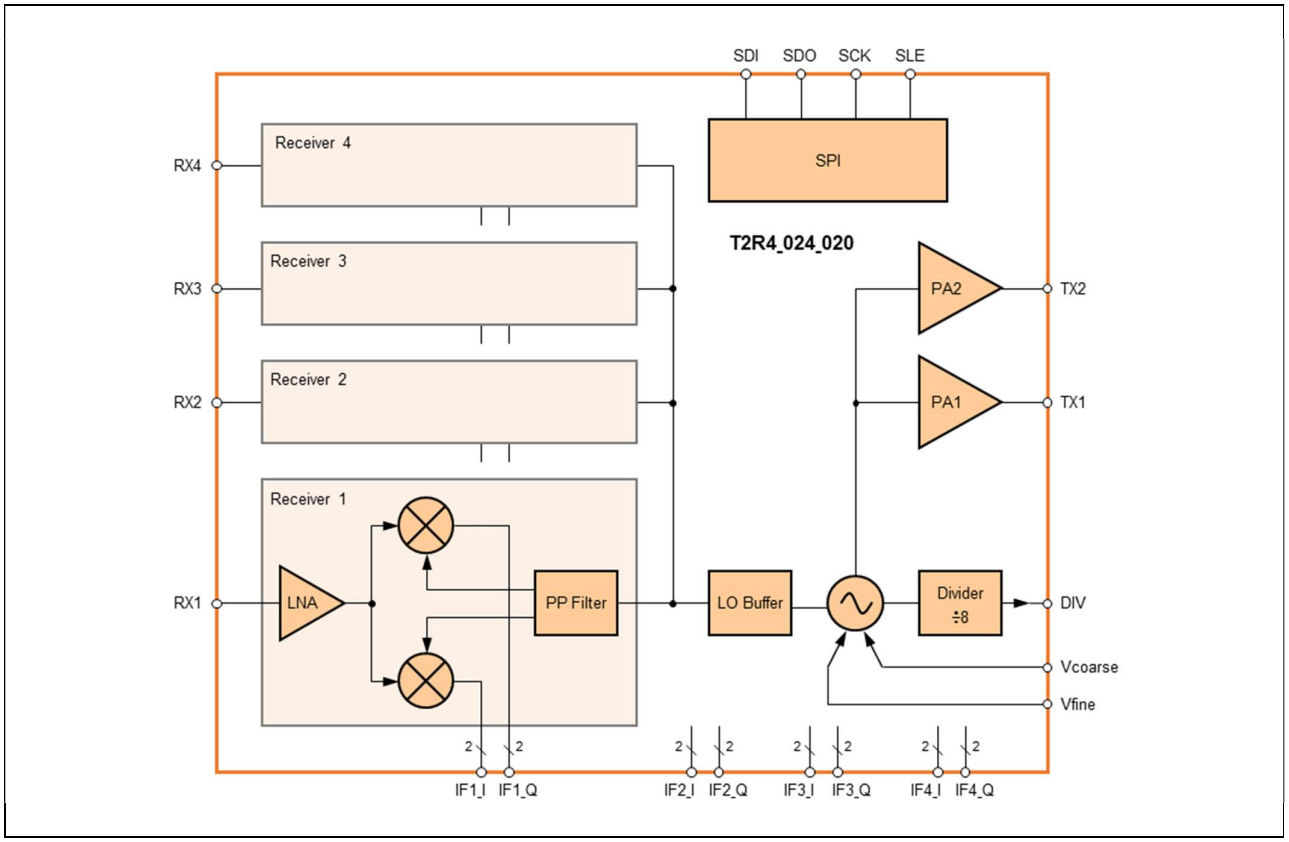

Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

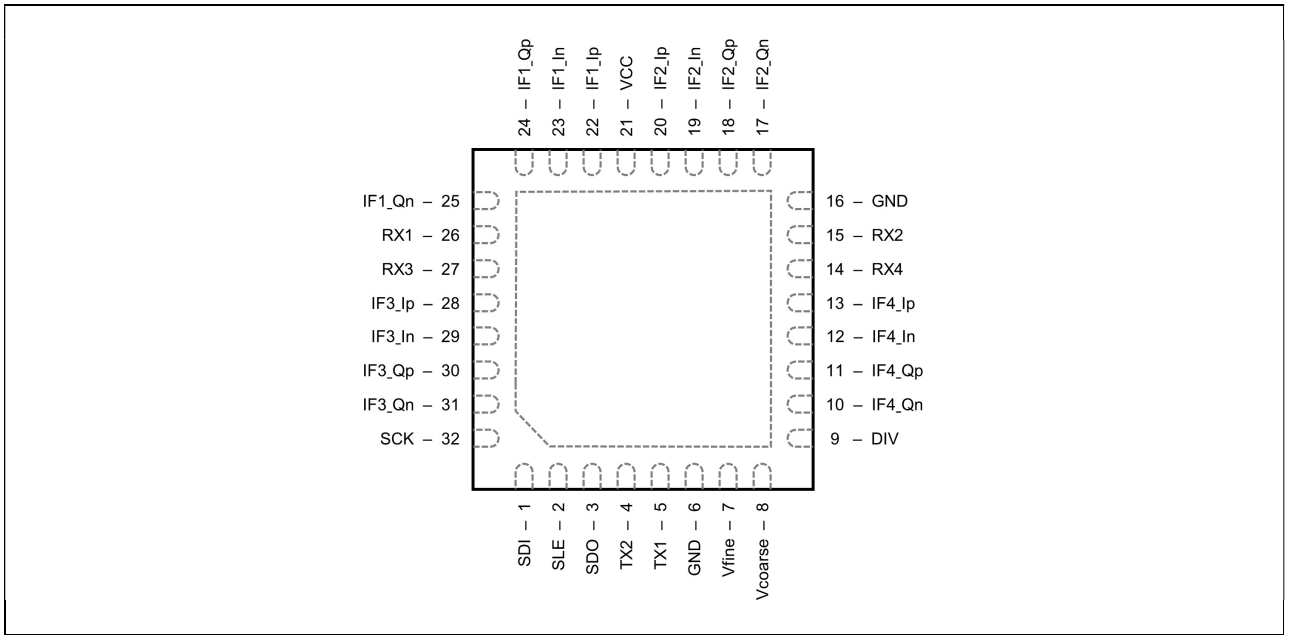

Figure 2 Pin Assignment (QFN32, 5 mm × 5 mm, top view)

3.2 Pin Description

Table 1 Pin Description

Pin		Description
No.	Name	
1	SDI	Serial data input of SPI interface
2	SLE	Latch enable input of SPI interface
3	SDO	Serial data output of SPI interface
4	TX1	Transmitter 1 output, 50 Ω
5	TX2	Transmitter 2 output, 50 Ω
6	GND	Ground
7	Vfine	Fine tuning of VCO, analog control voltage input with internal 120-kΩ pull-up resistor
8	Vcoarse	Coarse tuning of VCO, analog control voltage input with internal 40-kΩ pull-up resistor
9	DIV	÷8 divider output, 50 Ω, DC coupled
10	IF4_Qn	IF outputs of quadrature receiver 4, DC coupled, external AC coupling capacitors required.
11	IF4_Qp	
12	IF4_In	
13	IF4_Ip	
14	RX4	Receiver 4 input, 50 Ω
15	RX2	Receiver 2 input, 50 Ω
16	GND	Ground
17	IF2_Qn	IF outputs of quadrature receiver 2, DC coupled, external AC coupling capacitors required.
18	IF2_Qp	
19	IF2_In	
20	IF2_Ip	
21	VCC	Supply voltage (3.3 V)
22	IF1_Ip	IF outputs of quadrature receiver 1, DC coupled, external AC coupling capacitors required.
23	IF1_In	
24	IF1_Qp	
25	IF1_Qn	
26	RX1	Receiver 1 input, 50 Ω
27	RX3	Receiver 3 input, 50 Ω
28	IF3_Ip	IF outputs of quadrature receiver 3, DC coupled, external AC coupling capacitors required.
29	IF3_In	
30	IF3_Qp	
31	IF3_Qn	
32	SCK	Serial Clock Input of SPI interface
(33)	GND	Exposed die attach pad of the QFN package, must be soldered to ground.

4 Specification

4.1 Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only given within the operational specifications, not at absolute maximum ratings.

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Condition / Remark
Supply Voltage	V_{CC}		3.6	V	to GND
DC voltage at RF pins	V_{DCRF}	0	2	mV	IC provides low ohmic circuit to GND for TXout and RXin
Junction temperature	T_J		150	°C	
Storage temperature range	T_{STG}	-65	150	°C	
DC voltage at control inputs	V_{CTL}	-0.3	V_{CC} + 0.3	V	Vfine, Vcoarse
DC voltage at logic inputs	V_{IN}	-0.3	V_{CC} + 0.3	V	SDI, SLE, SDO, SCK
Input power into pin RFin	P_{IN}		0	dBm	
ESD robustness [1)]	V_{ESD}		500	V	Class 1A [1)]

1) According to ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing, Human Body Model Component Level, ANSI/ESDA/JEDEC JS-001-2011

4.2 Operating Range

Table 3 Operating Range

Parameter	Symbol	Min	Max	Unit	Condition / Remark
Ambient temperature	T_A	-40	85	°C	
Supply voltage	V_{CC}	3.13	3.47	V	(3.3V ± 5%)
DC voltage at control inputs	V_{CTL}	0	V_{CC}	V	Vfine, Vcoarse
DC voltage at logic inputs	V_{IN}	0	V_{CC}	V	SDI, SLE, SDO, SCK

Note: Do not drive input signals without power supplied to the device.

4.3 Thermal Resistance

Table 4 Thermal Resistance

Parameter	Symbol	Min	Typ	Max.	Unit	Condition / Remark
Thermal resistance, junction-to-ambient	R_{thja}			50	K/W	JEDEC standard JESD-51-5

5 Electrical Characteristics

T_A = -40 °C ~ +85 °C unless otherwise noted. Typical values measured at T_A = 25 °C and V_{CC} = 3.3 V.

Table 5 Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Condition / Remark
DC Parameters						
Supply current	I_{CC}		130		mA	4RX, TX, and divider enabled
Transmitter Section TX						
Transmitter start frequency	f_{TX}		22.7		GHz	
Transmitter stop frequency			26.3		GHz	
Divider division ratio	D_{div_o}		8			
Divider output frequency	f_{div_o}	2.83		3.28	GHz	
Tuning voltage VCO	V_{ctrl}	0		3.3	V	Vfine and Vcoarse
Tuning slope VCO (Vfine)	$\Delta f_{TX}/\Delta V_{ctrl}$		340		MHz/V	Only Vfine swept
Tuning slope VCO (Vcoarse)	$\Delta f_{TX}/\Delta V_{ctrl}$		1.18		GHz/V	Only Vcoarse swept
Tuning slope VCO (Vfine+Vcoarse)	$\Delta f_{TX}/\Delta V_{ctrl}$		1.71		GHz/V	Vfine and Vcoarse swept
Pushing VCO	$\Delta f_{TX}/\Delta V_{CC}$		135		MHz/V	f = 24.15 GHz
Phase noise	P_N		-102	-105	dBc/Hz	at 1 MHz offset
Output impedance	Z_{TXout}		50		Ω	
Transmitter output power	P_{TX}		6		dBm	
Adjustable range output power (TXp1 TXp1)	P_{TX_ADJ}	0		3.5	dBm	Power amplifier gain control 00 – TX off 01 – P_{OUT_MAX} – 3.5dB 10 – P_{OUT_MAX} – 3 dB 11 - P_{OUT_MAX}
Divider output power	P_{div_o}	-7	-5.5	-4	dBm	Note 1
Spurious power	P_{Sp-}		-45		dBm	f_{TX} - f_{div}
	P_{Sp+}		-43		dBm	f_{TX} + f_{div}
Harmonics power	P_{Ha12}		-46		dBm	12 GHz
	P_{Ha48}		-40		dBm	48 GHz
Receiver Section RX						
Receiver frequency	f_{RX}	22.3		26.9	GHz	
Receiver input impedance	Z_{RXIN}		50		Ω	
Number of adjustable gain modes			2			Adjustable LNA gain control
Gain high gain mode				16	dB	RXn_G = 1
Gain low gain mode				9	dB	RXn_G = 0
IF frequency range	f_{IF}	0		200	MHz	
IF output impedance	Z_{OUT}		500		Ω	Differential
IQ amplitude imbalance			1.0		dB	
IQ phase balance			10		deg	
Noise figure (DSB) high gain mode			4		dB	Simulated (double side band at f_{IF} = 1 MHz)
Noise figure (DSB) low gain mode			6		dB	Simulated
Input compression point	1dB ICP	-20		-13	dBm	

1) Divider output are loaded with 50 Ω, DC coupled, external decoupling capacitor ≥ 100 pF required.

6 SPI Interface

6.1 SPI Register

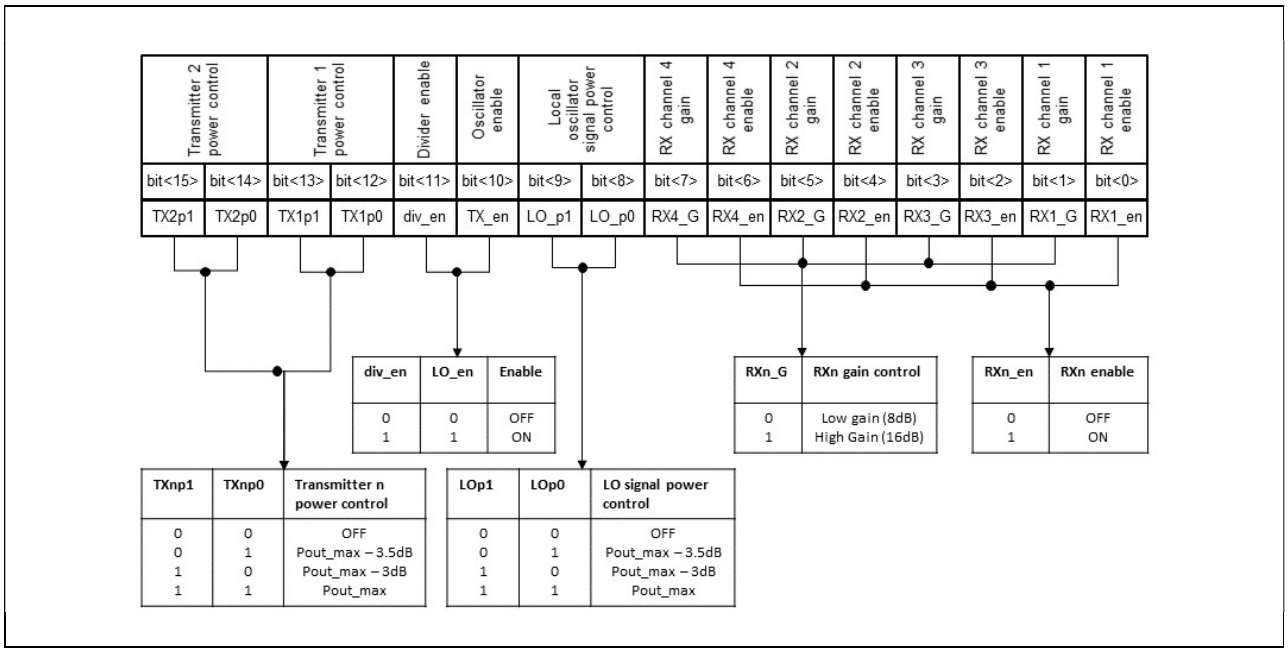

Figure 3 SPI Register Map

6.2 SPI Timing

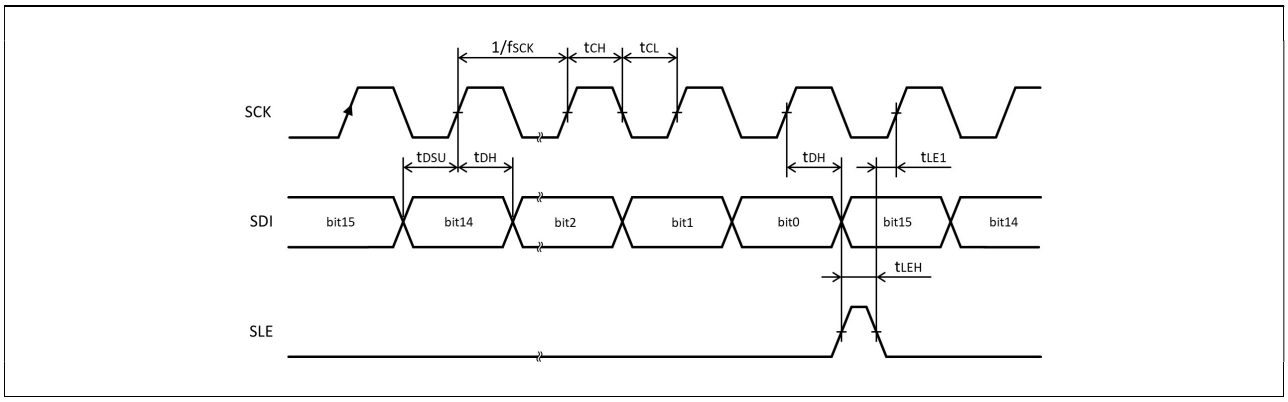

Figure 4 SPI Timing Diagram

Table 6 SPI Timing

Parameter	Symbol	Min	Typ	Max	Unit	Condition / Remark
SCK frequency	f_{SCK}			5	MHz	
Width of SCK high pulse	t_{CH}	100			ns	
Width of SCK low pulse	t_{CL}	100			ns	
SDI setup time	t_{DSU}	25			ns	
SDI hold time	t_{DH}	25			ns	
SLE pulse width	t_{LEH}	50			ns	
SLE low before SCK high	t_{LE1}	50			ns	

7 Packaging

7.1 Package Dimensions

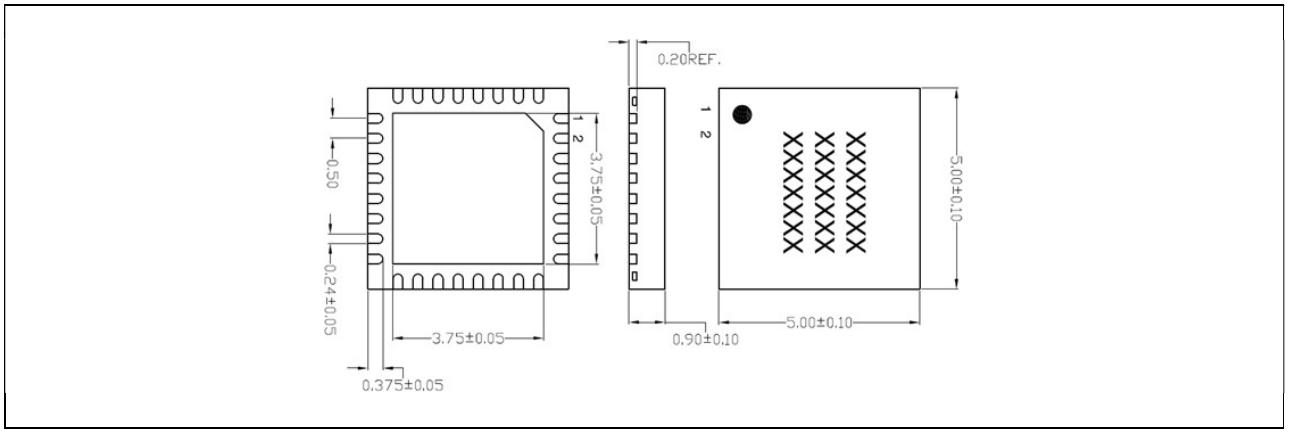

Figure 5 Outline Dimensions of QFN32 Package with Exposed Pad

IC Weight: 0.235g (typ.)

7.2 Package Code

Top-Side Markings TRX009
YYWW

7.3 Qualification Test

Table 7 Reliability and Environmental Test

Qualification Test	JEDEC Standard	Condition	Pass / Fail
MSL3	J-STD-020E	Reflow simulation 3 times at 260°C	pass

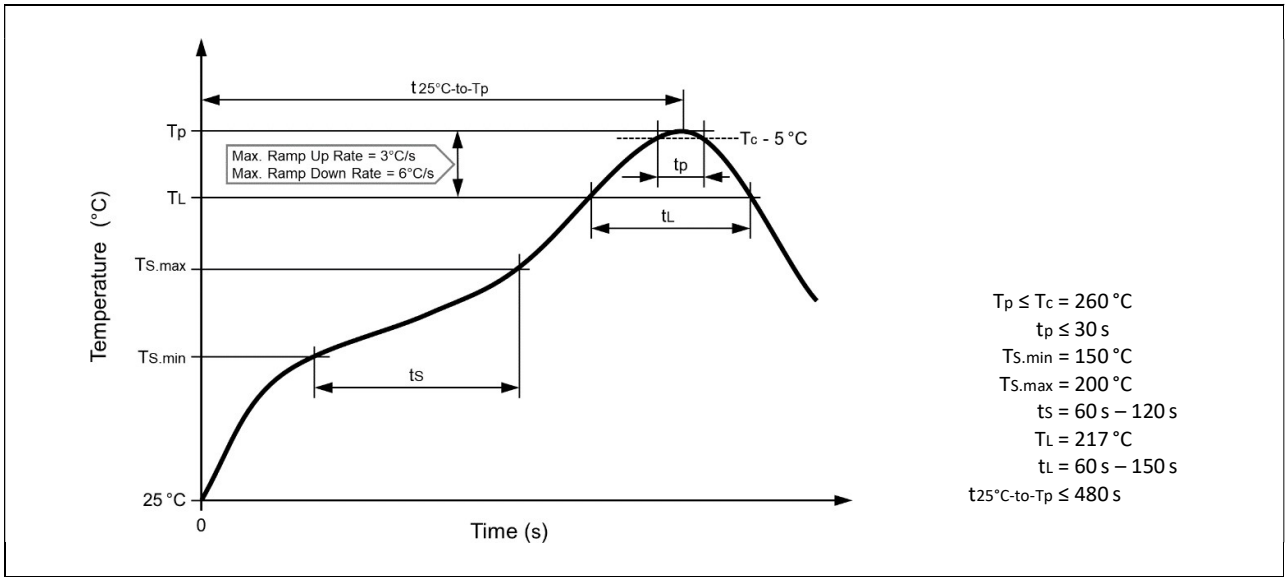

Figure 6 Reflow Profile for Pb-Free Assembly according to JEDEC Standard J-STD-020E

8 Application

8.1 Application Circuit Schematic

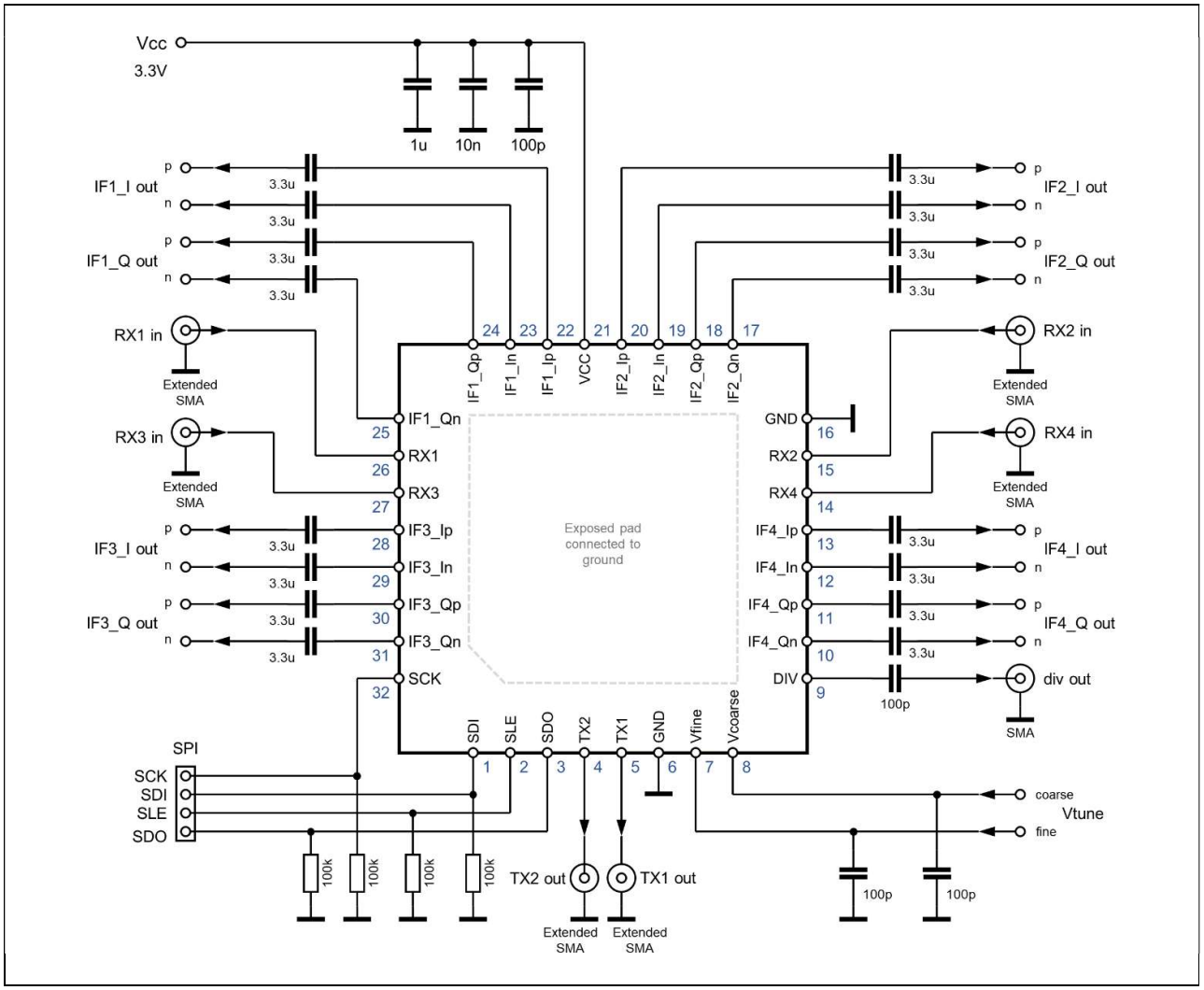

Figure 7 Application Circuit

8.2 Evaluation Board

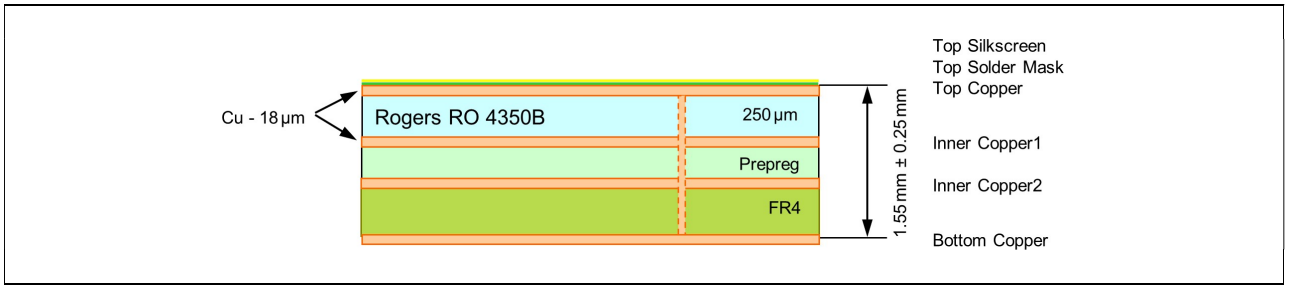

Figure 8 Evaluation Board Stack-Up

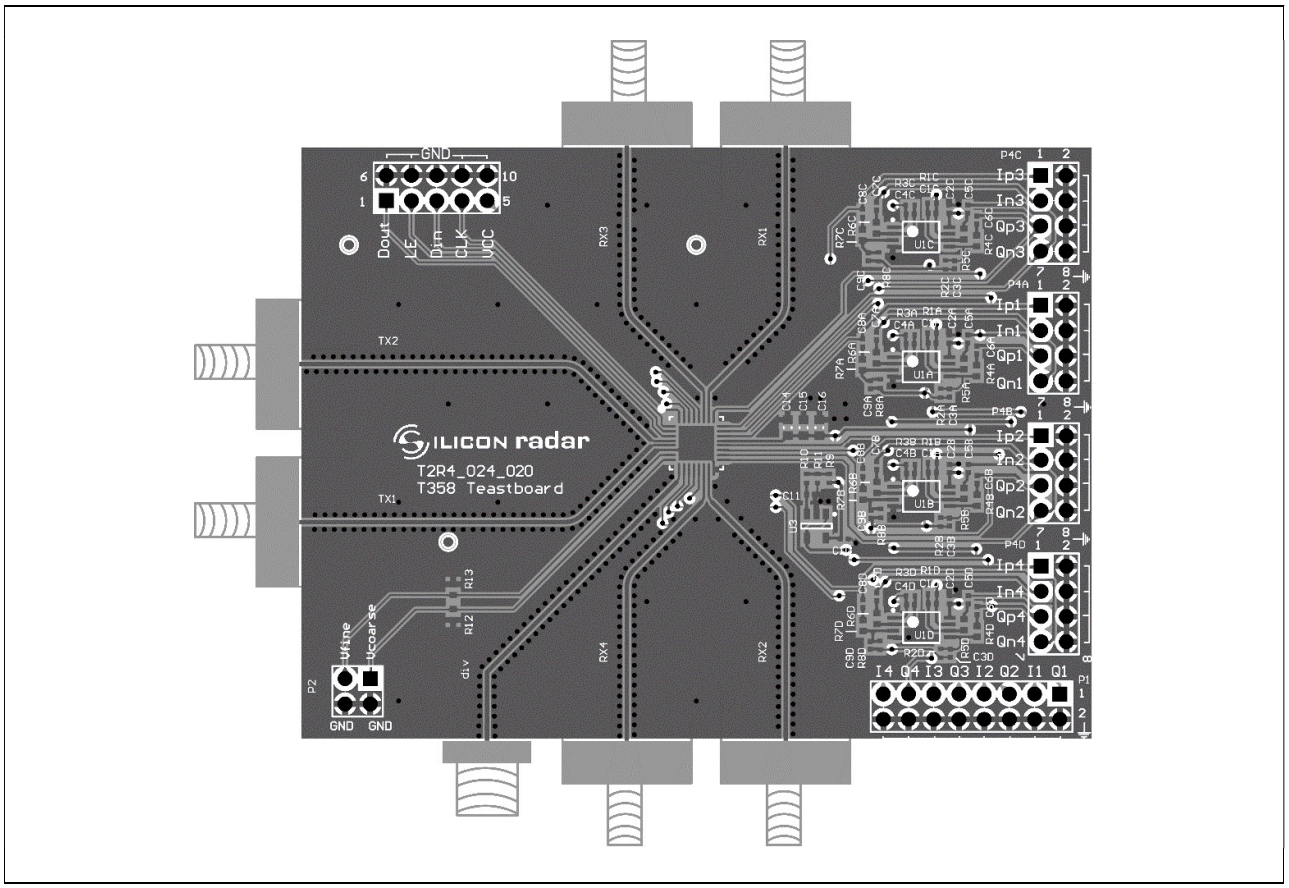

Figure 9 Evaluation Board Layout Including Via Holes (80 mm × 60 mm, top view)

8.3 Input / Output Stages

The following figures show the simplified circuits of the input and output stages.
It is important that the voltage applied to the input pins never exceeds VCC by more than 0.3 V. Otherwise, the supply current may be sourced through the upper ESD protection diode connected at the pin.

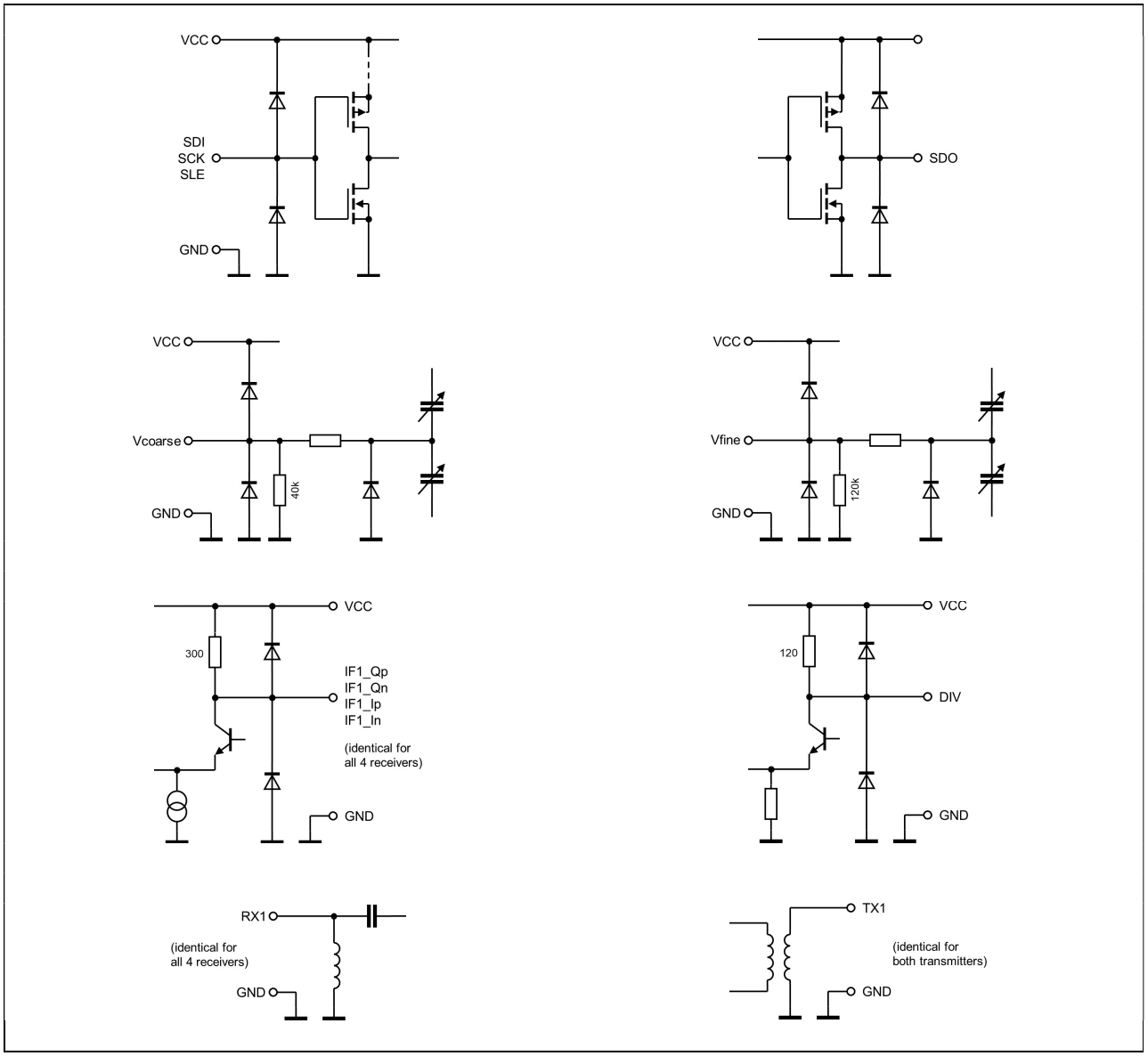

Figure 10 Equivalent I/O Circuits

9 Measurement Results

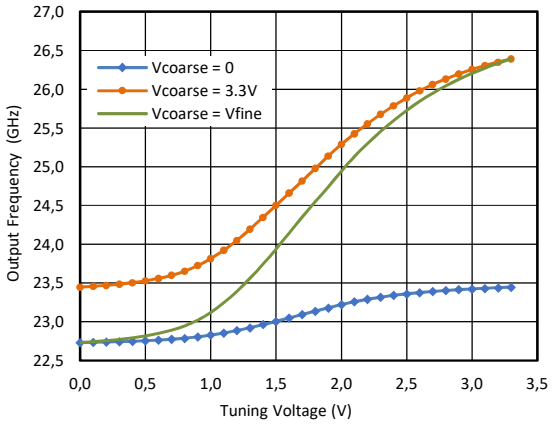

Figure 11 Output Frequency vs. Tuning Voltage, Vfine swept, Vcoarse parameter

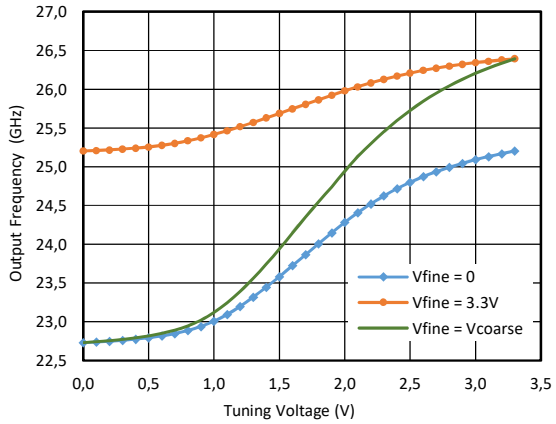

Figure 12 Output Frequency vs. Tuning Voltage, Vcoarse swept, Vfine parameter

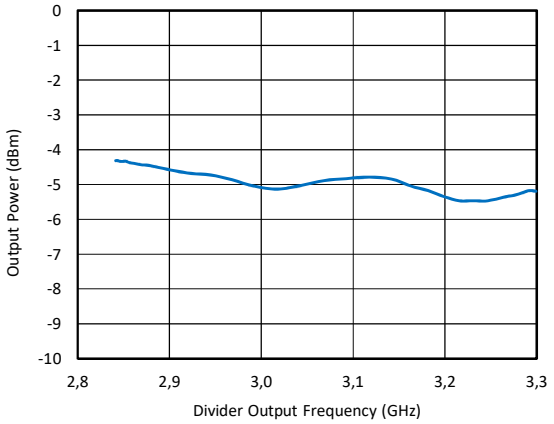

Figure 13 Divider Output Power vs. Divider Output Frequency

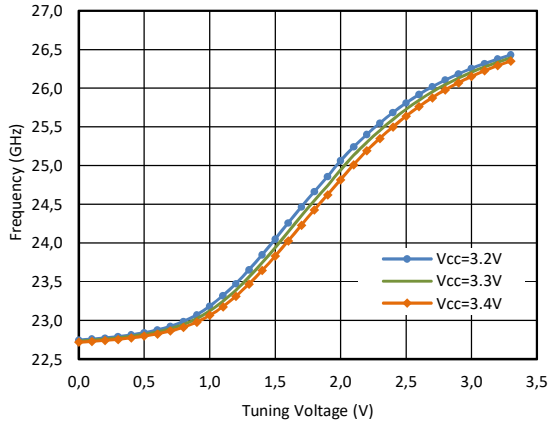

Figure 14 VCO Pushing ± 100mV
Vfine = Vcoarse swept, V_{CC} parameter

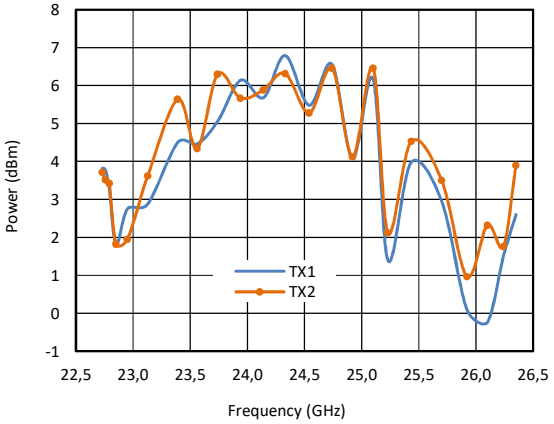

Figure 15 Transmitter Output Power vs. Frequency

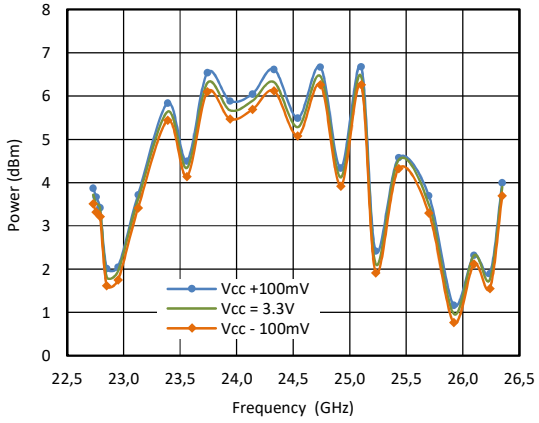

Figure 16 Vcc Pushing - Transmitter Output Power, SPI = FFFF

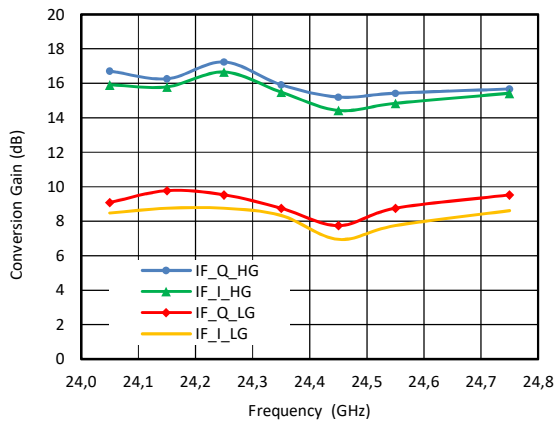

Figure 17 Receiver's Conversion Gain - ISM Band Frequency Range, parameter LNA gain: high gain (HG), low gain (LG)

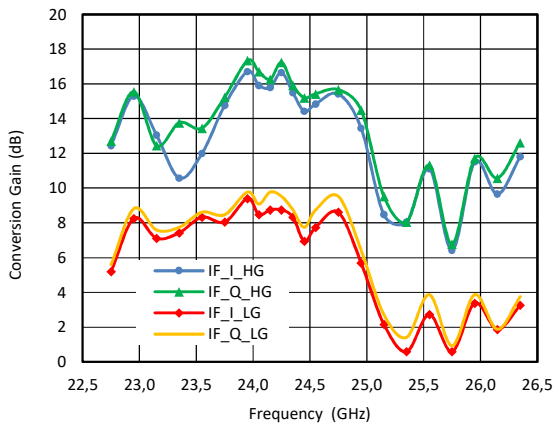

Figure 18 Receiver's Conversion Gain - Full Frequency Range, parameter LNA gain: high gain (HG), low gain (LG)

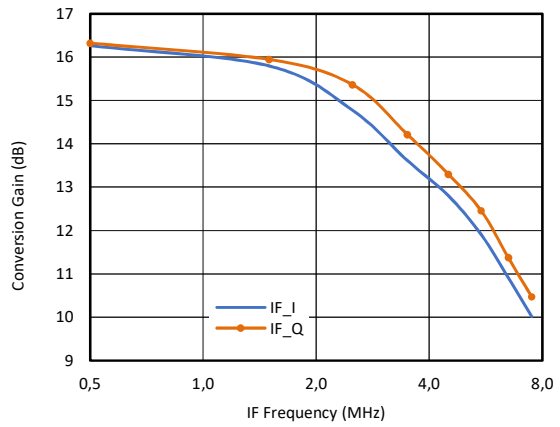

Figure 19 Conversion Gain vs. IF Frequency (cutoff frequency limited by measurement setup)

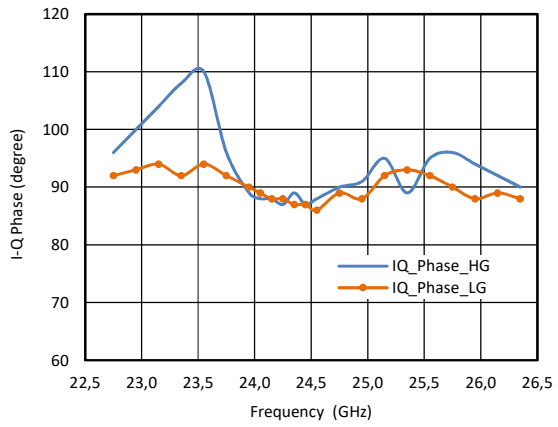

Figure 20 I-Q Phase vs. Output Frequency, parameter LNA gain: high gain (HG), low gain (LG)

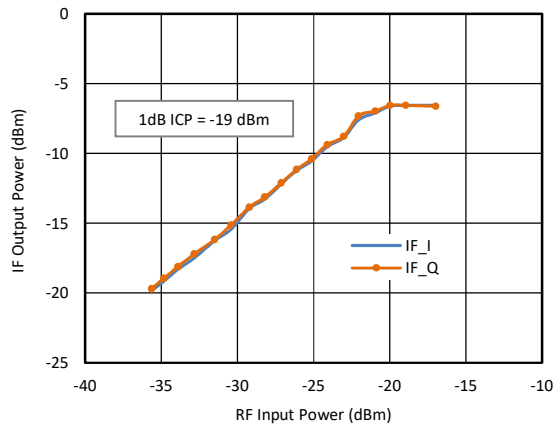

Figure 21 Linearity, high LNA gain

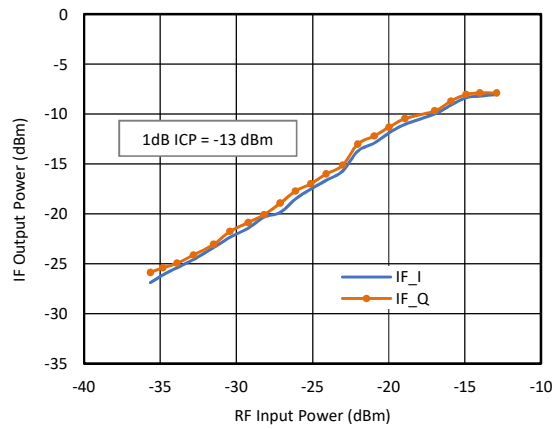

Figure 22 Linearity, low LNA gain

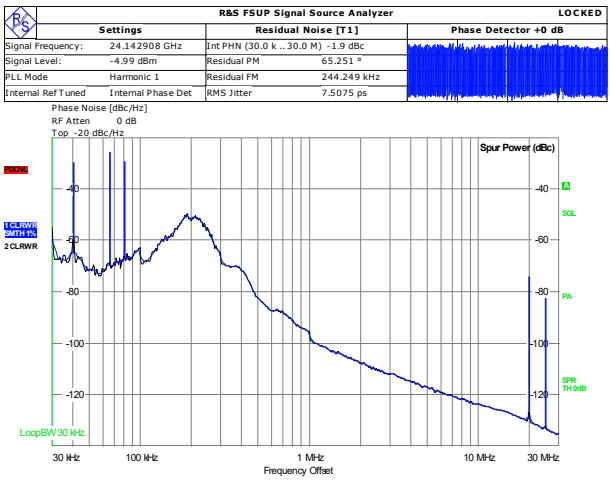

Figure 23 Phase Noise 24.14 GHz

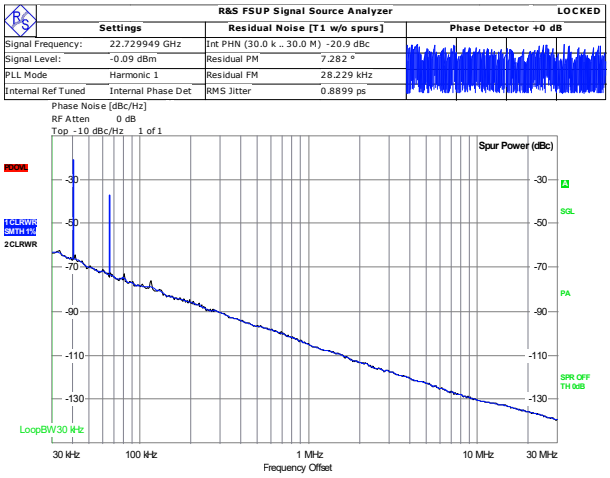

Figure 24 Phase Noise 22.7 GHz

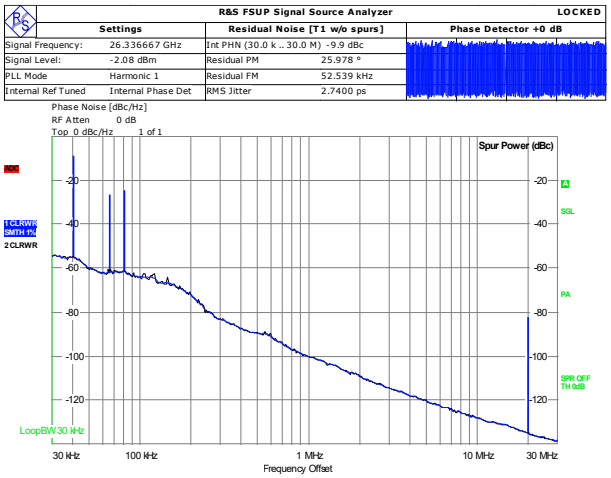

Figure 25 Phase Noise 26.3 GHz

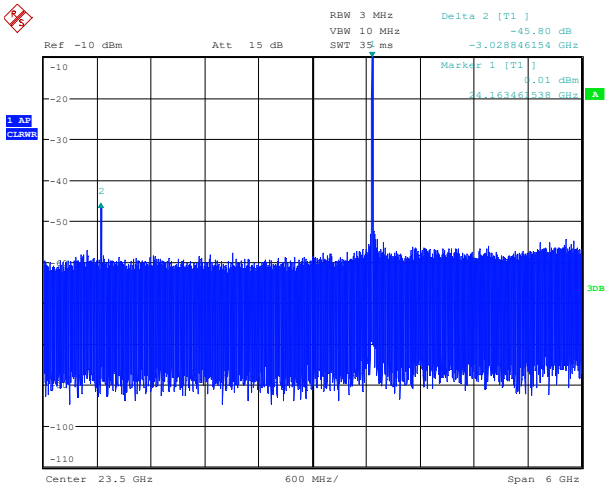

Figure 26 Transmitter Spectrum

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